WHAT IS CLAIMED IS:

1. A ternary content addressable memory ("CAM") cell comprising:

a main memory cell enabled to a wordline to store data;

a mask memory cell enabled to the wordline to store mask data;

a bitline pair for transmitting the data to or from the main memory cell;

a mask bitline pair for transmitting the mask data to the mask memory cell;

a comparison signal line pair for transmitting comparison data;

a match line;

a mask circuit for receiving the mask data, the mask circuit being coupled to the match line and the mask memory cell; and

a comparison circuit including a pair of transistors coupled to the comparison signal line pair and a pair of match transistors coupled to data of the main memory cell, the comparison circuit being coupled to a ground line of the mask circuit.

2. The ternary CAM cell of claim 1, characterized in that the comparison circuit includes:

a first NMOS transistor having a drain coupled to the mask circuit and a gate coupled to the comparison data;

a second NMOS transistor having a drain coupled to the mask circuit and a gate coupled to a comparison data line;

a first match NMOS transistor having a drain coupled to the first NMOS transistor, a gate coupled to the data of the main memory cell, and a source coupled to a ground voltage; and

a second match NMOS transistor having a drain coupled to the second NMOS transistor, a gate coupled to complementary data of the main memory cell, and a source coupled to a ground voltage.

3. The ternary CAM cell of claim 1, characterized in that the comparison circuit includes:

a first match NMOS transistor having a drain coupled to the mask circuit and a gate coupled to the data of the main memory cell;

a second match NMOS transistor having a drain coupled to the mask circuit and a gate coupled to the complementary data of the main memory cell;

a first NMOS transistor having a drain coupled to a source of the first NMOS transistor, a gate coupled to the comparison signal line, and a source coupled to a ground voltage; and

a second NMOS transistor having a drain coupled to a source of the second NMOS transistor, a gate coupled to the comparison signal line, and a source coupled to a ground voltage.

4. The ternary CAM cell of claim 1, characterized in that the mask circuit is an NMOS transistor which is coupled between the match line and

the comparison circuit and is gated by the mask data.

5. A ternary content addressable memory ("CAM") cell comprising:

a main memory cell enabled to a wordline to store data;

a mask memory cell enabled to the wordline to store mask data;

a bitline pair for transmitting the data to or from the main memory cell;

a mask bitline pair for transmitting the mask data to the mask memory cell;

a comparison signal line pair for transmitting comparison data;

a match line;

a mask circuit for receiving the mask data, the mask circuit being coupled to the mask memory cell; and

a comparison circuit including a pair of transistors coupled to the comparison signal line pair and a pair of match transistors coupled to data of the main memory cell, the comparison circuit being coupled between the match line and the mask circuit

6. The ternary CAM cell of claim 5, characterized in that the comparison circuit includes:

a first NMOS transistor having a drain coupled to the match line and a gate coupled to the comparison data line;

a second NMOS transistor having a drain coupled to the match line and a gate coupled to a complementary comparison data line;

a first match NMOS transistor having a drain coupled to a source of the first NMOS transistor and a gate coupled to the data of the main memory cell; and

a second match NMOS transistor having a drain coupled to a source of the second NMOS transistor, a gate coupled to complementary data of the main memory cell, and a source coupled to a source of the main memory cell.

7. The ternary CAM cell of claim 5, characterized in that the comparison circuit includes:

a first match NMOS transistor having a drain coupled to the match line and a gate coupled to the data of the main memory cell;

a second match NMOS transistor having a drain coupled to the match line and a gate coupled to the complementary data of the main memory cell;

a first NMOS transistor having a drain coupled to a source of the first match NMOS transistor and a gate coupled to the comparison signal line; and

a second NMOS transistor having a drain coupled to a source of the second match NMOS transistor, a gate coupled to a complementary comparison signal line, and a source coupled to a source of the first NMOS transistor.

8. The ternary CAM cell of claim 5, characterized in that the mask circuit is an NMOS transistor which is coupled between the match line and the comparison circuit and is gated by the mask data.

9. A ternary content addressable memory ("CAM") cell comprising:

a wordline;

a main memory cell in signal communication with the wordline for storing data;

a bitline pair in signal communication with the main memory cell for transmitting data to or from the main memory cell;

a mask memory cell in signal communication with the wordline for storing mask data;

a mask bitline pair in signal communication with the mask memory cell for transmitting mask data to the mask memory cell;

a comparison circuit in signal communication with the main memory cell and the mask circuit;

a comparison signal line pair in signal communication with the comparison circuit for transmitting comparison data;

a mask circuit in signal communication with the mask memory cell and the comparison circuit for receiving the mask data; and

a match line in signal communication with at least one of the mask circuit and the comparison circuit.

10. The ternary CAM cell of Claim 9, the comparison circuit comprising a pair of transistors coupled to the comparison signal line pair and a pair of match transistors coupled to data of the main memory cell.

11. The ternary CAM cell of Claim 9 wherein the comparison circuit is in signal communication with a ground line of the mask circuit.

12. The ternary CAM cell of Claim 9 wherein the comparison circuit is in signal communication between the match line and the mask circuit.

13. The ternary CAM cell of Claim 9, the comparison circuit comprising:

a first NMOS transistor having a drain coupled to the mask circuit and a gate coupled to a complimentary comparison data line of the comparison signal line pair;

a second NMOS transistor having a drain coupled to the mask circuit and a gate coupled to a comparison data line of the comparison signal line pair;

a first match NMOS transistor having a drain coupled to the first NMOS transistor, a gate coupled to the data of the main memory cell, and a source coupled to a ground voltage; and

a second match NMOS transistor having a drain coupled to the second NMOS transistor, a gate coupled to complementary data of the main memory cell, and a source coupled to a ground voltage.

14. The ternary CAM cell of Claim 9, the comparison circuit

comprising:

a first match NMOS transistor having a drain coupled to the mask circuit and a gate coupled to the data of the main memory cell;

a second match NMOS transistor having a drain coupled to the mask circuit and a gate coupled to the complementary data of the main memory cell;

a first NMOS transistor having a drain coupled to a source of the first match NMOS transistor, a gate coupled to a complementary comparison signal line of the comparison signal line pair, and a source coupled to a ground voltage; and

a second NMOS transistor having a drain coupled to a source of the second match NMOS transistor, a gate coupled to the comparison signal line of the comparison signal line pair, and a source coupled to a ground voltage.

15. A ternary content addressable memory ("CAM") cell comprising:

wordline means for transmitting a word signal;

main memory cell means in signal communication with the wordline means for storing data;

bitline pair means in signal communication with the main memory cell means for transmitting data to or from the main memory cell means;

mask memory cell means in signal communication with the wordline means for storing mask data;

mask bitline pair means in signal communication with the mask

memory cell means for transmitting mask data to the mask memory cell means;

comparison circuit means in signal communication with the main memory cell means and the mask circuit means;

comparison signal line pair means in signal communication with the comparison circuit means for transmitting comparison data;

mask circuit means in signal communication with the mask memory cell means and the comparison circuit means for receiving the mask data; and

match line means in signal communication with at least one of the mask circuit means and the comparison circuit means.

16. The ternary CAM cell of Claim 15, the comparison circuit means comprising a pair of switching means coupled to the comparison signal line pair means and a pair of match switching means coupled to data of the main memory cell means.

17. The ternary CAM cell of Claim 15 wherein the comparison circuit means is in signal communication with a grounding means of the mask circuit means.

18. The ternary CAM cell of Claim 15 wherein the comparison circuit means is in signal communication between the match line means and the mask circuit means.

19. The ternary CAM cell of Claim 15, the comparison circuit means comprising:

a first switching means having a drain coupled to the mask circuit means and a gate coupled to a complimentary comparison data line of the comparison signal line pair means;

a second switching means having a drain coupled to the mask circuit means and a gate coupled to a comparison data line of the comparison signal line pair means;

a first match switching means having a drain coupled to the first switching means, a gate coupled to the data of the main memory cell means, and a source coupled to a grounding means; and

a second match switching means having a drain coupled to the second switching means, a gate coupled to complementary data of the main memory cell means, and a source coupled to a grounding means.

20. The ternary CAM cell of Claim 15, the comparison circuit means comprising:

a first match switching means having a drain coupled to the mask circuit means and a gate coupled to the data of the main memory cell means;

a second match switching means having a drain coupled to the mask circuit means and a gate coupled to the complementary data of the main memory cell means;

a first switching means having a drain coupled to a source of the first match switching means, a gate coupled to a complementary comparison signal line of the comparison signal line pair means, and a source coupled to a grounding means; and

a second switching means having a drain coupled to a source of the second match switching means, a gate coupled to the comparison signal line of the comparison signal line pair means, and a source coupled to a grounding means.